IN THE CLAIMS

Please amend the claims to read as follows:

Listing of Claims

1. (Canceled).

2. (Currently Amended) A microcontroller having a processor receiving as a system clock a clock signal corresponding to frequency information among a plurality of clock signals of different frequencies that are each 1/n (n is a division ratio and an integer not less than 1) an oscillation frequency, operating in synchronism with the system clock, performing fetching and decoding of an extension code, an operation code and an operand stored in a memory by pipeline processing, on an instruction program comprising the extension code, the operation code and the operand, and executing the instruction program based on a result of the decoding,

wherein the operation code is structured, by a machine code, as an instruction map comprising a plurality of pages which instruction map is classified into pages each corresponding to a division ratio,

wherein the extension code pipeline-processed together with the operation code is provided with information representative of a page of the instruction map, ~~and~~

wherein the processor outputs the frequency information corresponding to the division ratio corresponding to the page of the instruction map represented by the extension code by fetching and decoding the extension code by pipeline processing, and

wherein a selector is provided that selects the extension code corresponding to the division ratio in accordance with a division ratio setting description determining the division ratio of the system clock described in a source program, selects the operation code corresponding to an instruction succeeding the division ratio setting description from the page of the instruction map represented by the extension code, and converts it into a ROM code.

3. (Canceled).

4. (Original) A microcontroller according to claim 2, wherein a clock generator is provided that generates the plurality of clock signals of different frequencies that are each 1/n (n is a division ratio and an integer not less than 1) the oscillation frequency, selects from among the clock signals a

clock signal corresponding to the frequency information outputted from the processor, and outputs the selected clock signal as the system clock to the processor.

5. (Canceled).

6. (Currently Amended) A microcontroller according to claim 4, wherein the clock generator comprises:

a divider that outputs ~~dividing means for outputting~~ the plurality of clock signals of the different frequencies that are 1/n (n is a division ratio and an integer not less than 1) the oscillation frequency;

a clock signal selector that selects ~~selecting means for selecting~~ one clock signal based on a selection signal from among the plurality of clock signals outputted by the divider ~~dividing means~~, and ~~outputting~~ outputs the selected clock signal as the system clock; and

a controller that outputs ~~control means for outputting~~ the selection signal corresponding to the frequency information outputted from the processor, to the clock signal selector ~~selecting means~~.

7. (Currently Amended) A microcontroller having a processor receiving as a system clock a clock signal corresponding to frequency information among a plurality of clock signals of different frequencies that are each 1/n (n is a division ratio and an integer not less than 1) an oscillation frequency, operating in synchronism with the system clock, performing fetching and decoding of an operation code and an operand stored in a memory by pipeline processing, on an instruction program comprising the operation code and the operand, and executing the instruction program based on a result of the decoding, wherein the operation code to which a frequency control signal for determining the division ratio of the system clock is added is stored in the memory, and wherein the processor outputs the frequency information corresponding to the frequency control signal by fetching and decoding the frequency control signal together with the operation code by pipeline processing,

~~A microcontroller according to claim 1,~~

wherein ~~means~~ a frequency control signal generator is provided for generating the frequency control signal in accordance with a division ratio setting description determining the division ratio of the system clock described in a source program, adding the frequency control signal to the operation

code generated from an instruction succeeding the division ratio setting description, and converting it into a ROM code.

8. (Currently Amended) A microcontroller having a processor receiving as a system clock a clock signal corresponding to frequency information among a plurality of clock signals of different frequencies that are each 1/n (n is a division ratio and an integer not less than 1) an oscillation frequency, operating in synchronism with the system clock, performing fetching and decoding of an operation code and an operand stored in a memory by pipeline processing, on an instruction program comprising the operation code and the operand, and executing the instruction program based on a result of the decoding, wherein the operation code to which a frequency control signal for determining the division ratio of the system clock is added is stored in the memory, and wherein the processor outputs the frequency information corresponding to the frequency control signal by fetching and decoding the frequency control signal together with the operation code by pipeline processing,

~~A microcontroller according to claim 1,~~

wherein ~~means~~ a frequency control signal generator is provided for generating the frequency control signal in accordance with a division ratio setting description determining

the division ratio of the system clock described in a source program, adding the frequency control signal to the operation code generated from an instruction preceding the division ratio setting description when the number of execution cycles of the instruction preceding the division ratio setting description is less than a reference, adding the frequency control signal to the operation code generated from an instruction succeeding the division ratio setting description when the number of execution cycles is not less than the reference, and converting it into a ROM code.

9. (Canceled).